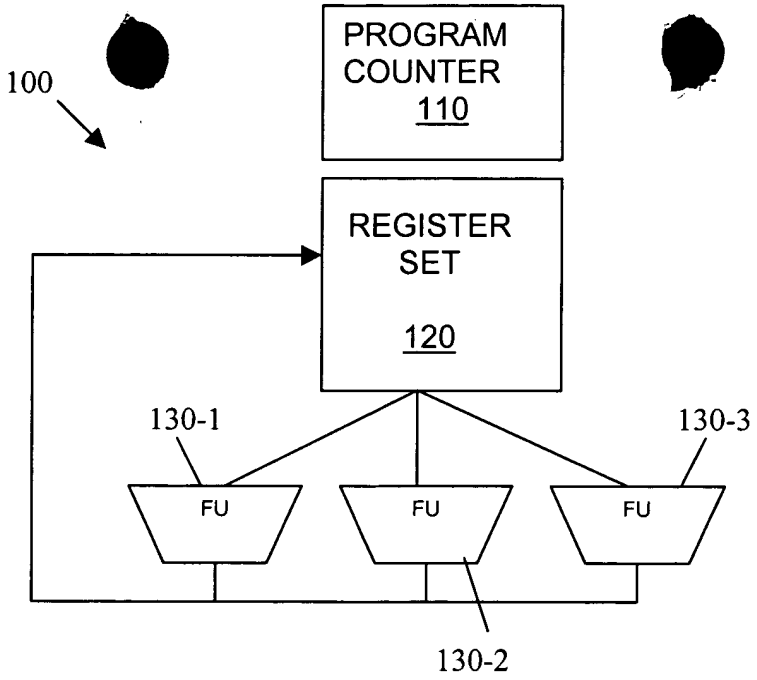

PRIOR ART

FIG. 1

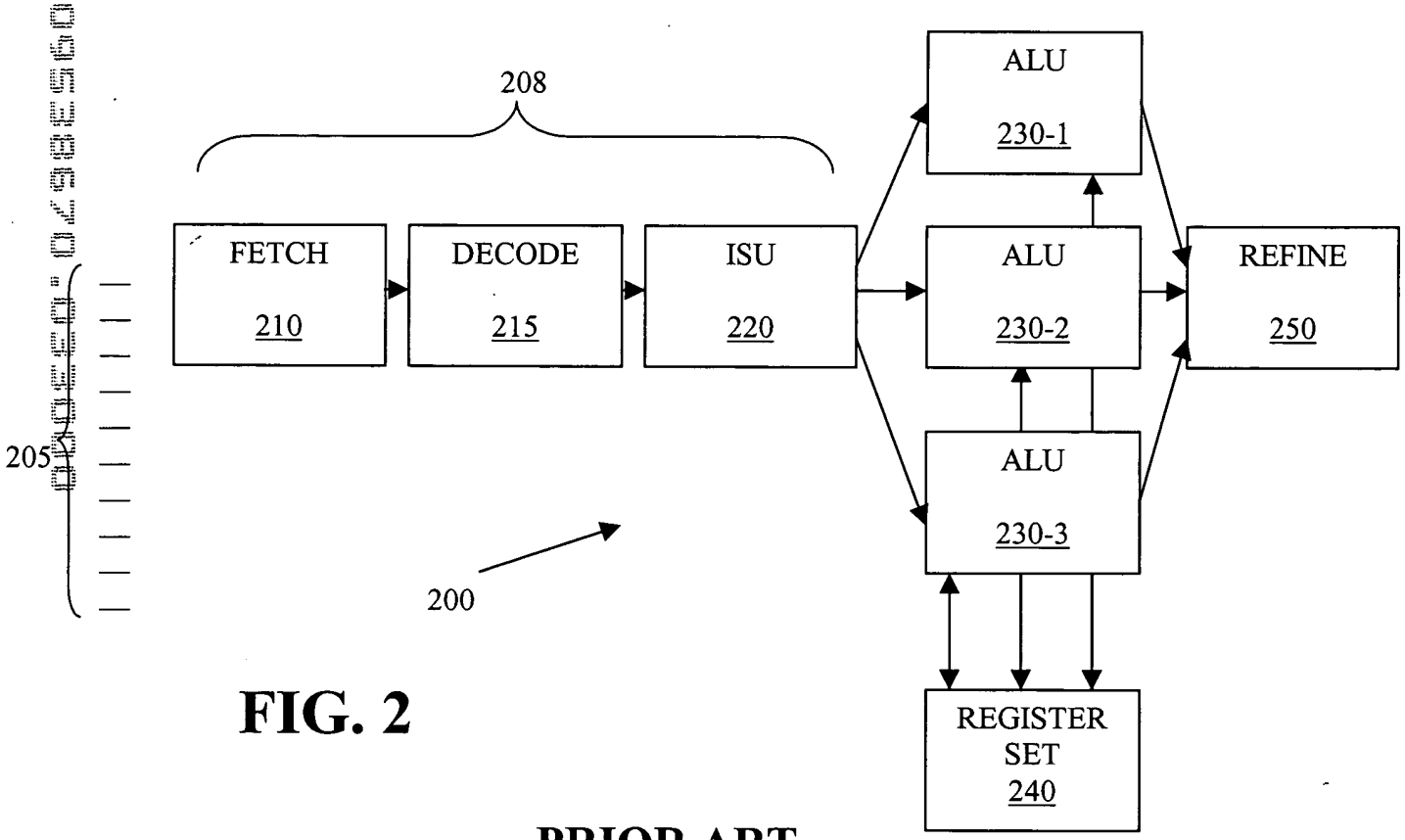

FIG. 2

PRIOR ART

```
310 {  L3:  ADD  R0, R1, R2
       L2:  SUB  R3, R4, R2
       L1:  OR   R6, R1, R5
```

FIG. 3

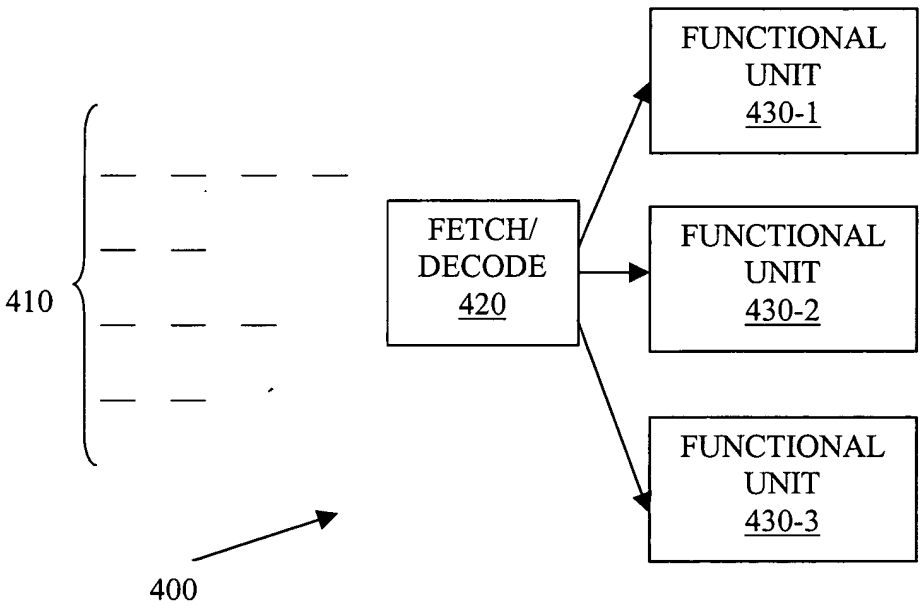

FIG. 4 PRIOR ART

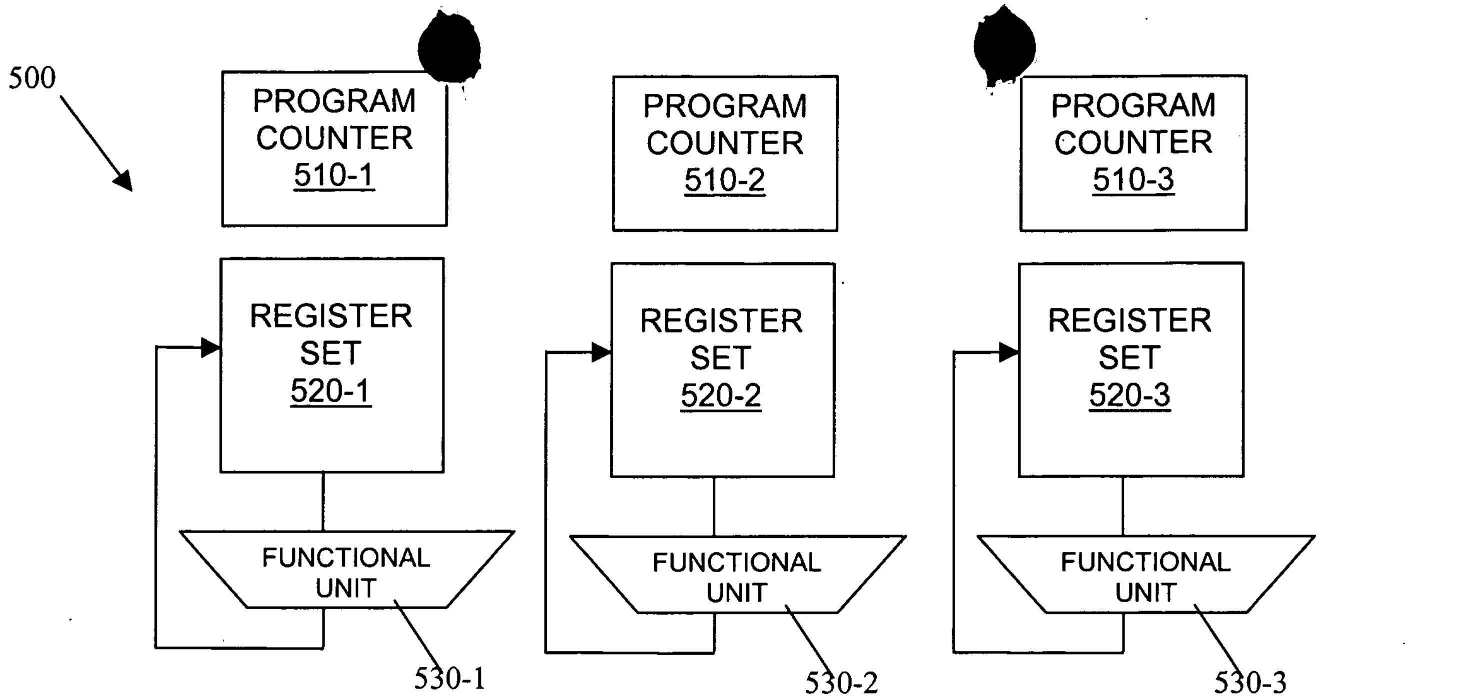

FIG. 5

PRIOR ART

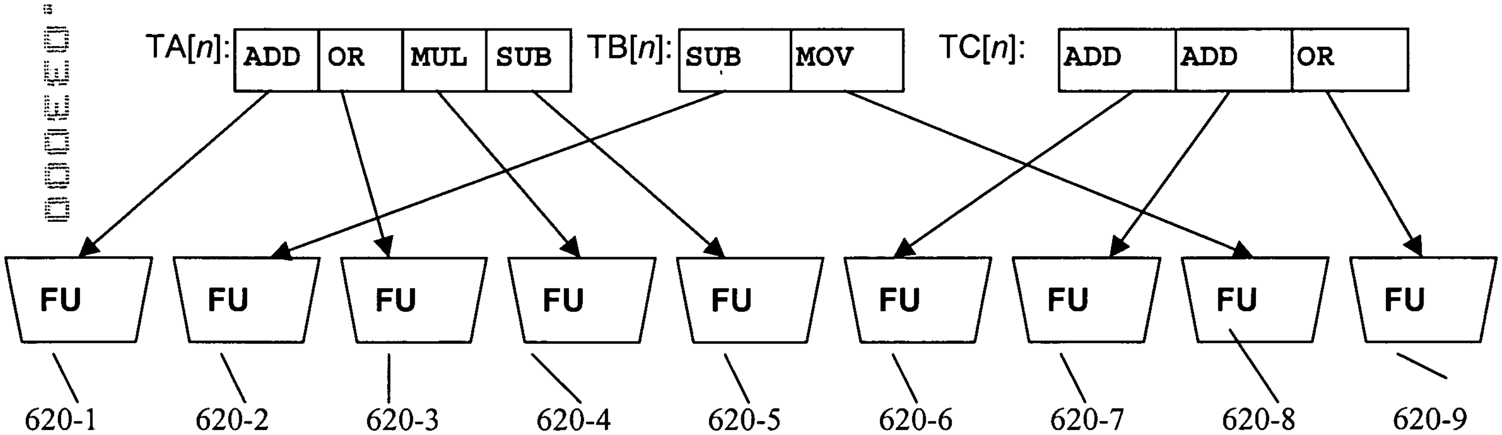

FIG. 6

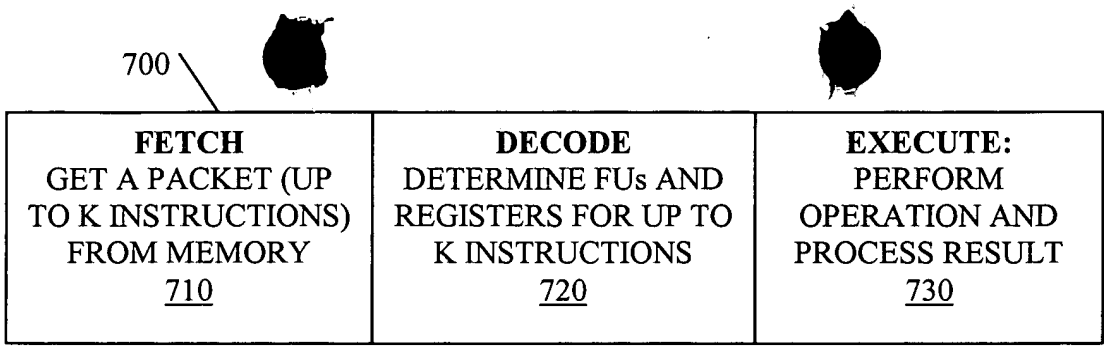

FIG. 7A PRIOR ART

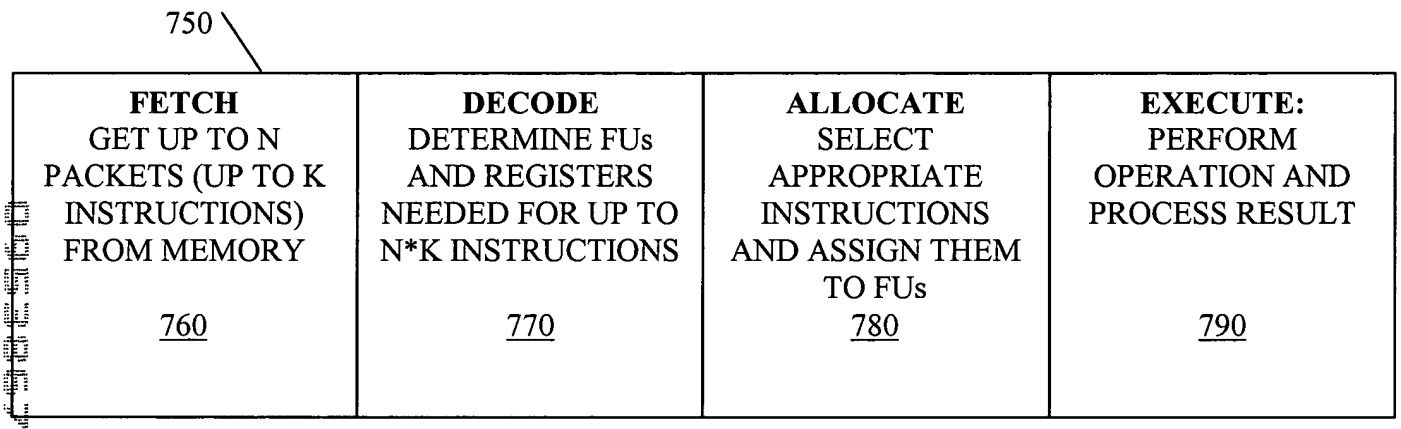

FIG. 7B

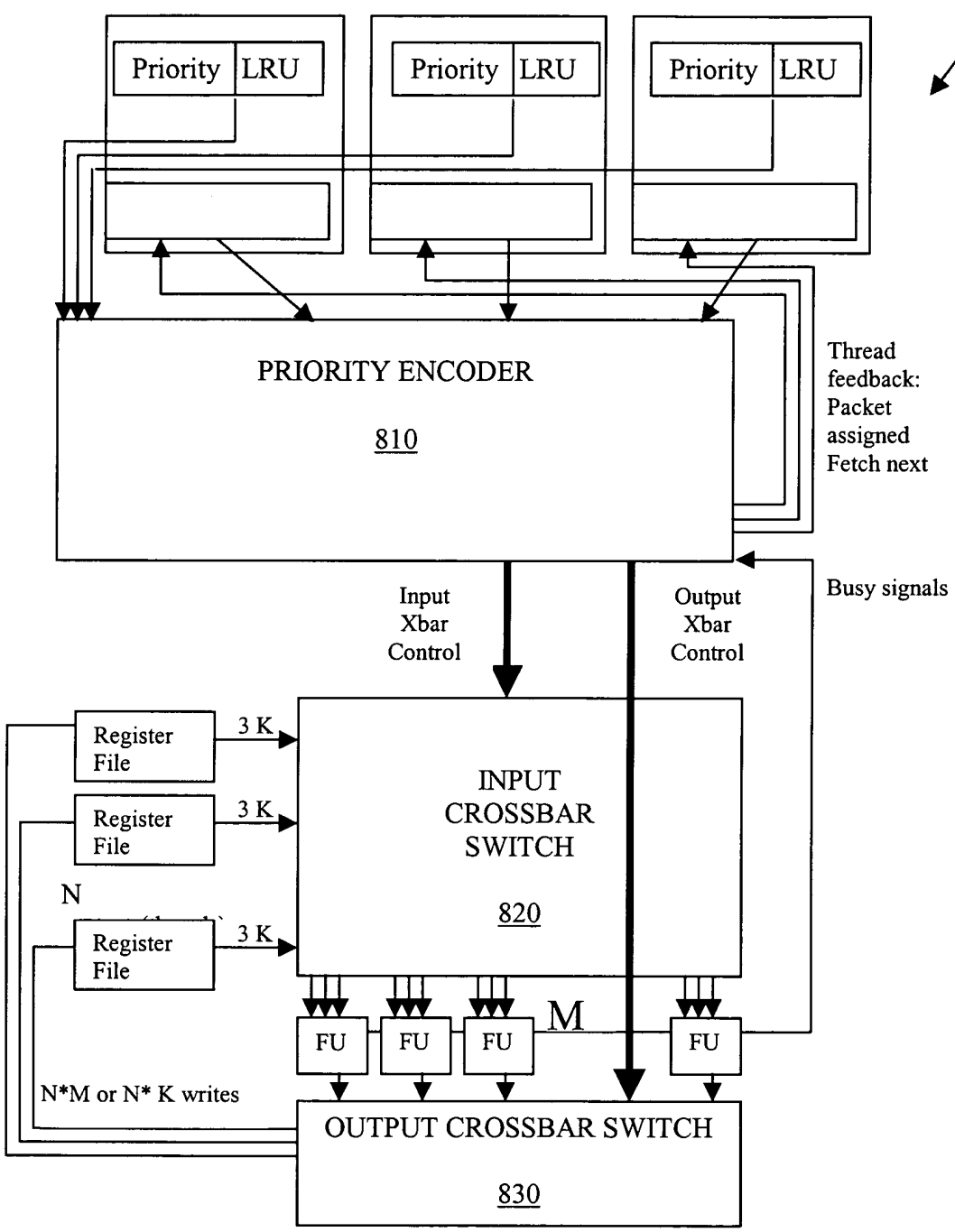
780
Priority
LRU
Priority
LRU
Priority
LRU
PRIORITY ENCODER
810
Thread feedback: Packet assigned Fetch next
Busy signals
Input Xbar Control
Output Xbar Control
Register File
3 K
Register File
3 K
N
Register File
3 K
INPUT CROSSBAR SWITCH
820
M
FU
FU
FU
FU
N*M or N* K writes
OUTPUT CROSSBAR SWITCH
830

FIG. 8